What is claimed is:

1. An apparatus comprising:
a power supply node;
a load circuit;
a transistor coupled between the power supply node and the load circuit; and
a control circuit to utilize the transistor as a regulator or a sleep transistor.

2. The apparatus of claim 1 wherein the control circuit includes an error amplifier to influence operation of the transistor.

3. The apparatus of claim 1 wherein the control circuit comprises a plurality of control loops to influence operation of the transistor as a regulator.

4. The apparatus of claim 3 wherein the control circuit comprises a first control loop having an error amplifier.

5. The apparatus of claim 4 wherein the control circuit further comprises a second control loop having a higher bandwidth than the first control loop.

6. The apparatus of claim 5 wherein the second control loop is adapted to sense a voltage between the transistor and the load circuit using a source of a second transistor.

7. The apparatus of claim 1 further comprising:
a second power supply node; and
a second transistor coupled between the load circuit and the second power supply node;
wherein the control circuit is adapted to utilize the second transistor as a regulator or a sleep transistor.

8. The apparatus of claim 1 wherein the load circuit comprises a memory circuit.

9. The apparatus of claim 1 wherein the load circuit comprises a cache memory circuit.

10. A circuit comprising a sleep transistor coupled between a power supply node and a load circuit, wherein the sleep transistor is coupled to provide power supply regulation.

11. The circuit of claim 10 further comprising an error amplifier coupled to the sleep transistor.

12. The circuit of claim 11 further comprising a multiplexer coupled between the error amplifier and the sleep transistor, wherein the multiplexer is adapted to conditionally turn off the sleep transistor.

13. The circuit of claim 10 further comprising a control circuit to conditionally turn off the sleep transistor.

14. The circuit of claim 13 wherein the control circuit comprises a first control loop including an error amplifier.

15. The circuit of claim 14 wherein the control circuit comprises a second control loop including a sensing transistor coupled to sense a voltage variation using a source terminal.

16. The circuit of claim 15 wherein the control circuit further comprises a bias transistor coupled between the sensing transistor and a second power supply node.

17. The circuit of claim 16 further comprising a voltage divider coupled between the power supply node and a node formed at a junction between the sensing transistor and bias transistor, the voltage divider to influence operation of the sleep transistor.

18. The circuit of claim 10 wherein the load circuit comprises a memory circuit.

19. The circuit of claim 10 wherein the load circuit comprises a cache memory circuit.

20. The circuit of claim 10 wherein the load circuit is in a first integrated circuit die, and the sleep transistor is in a second integrated circuit die.

21. The circuit of claim 20 wherein the first integrated circuit die is mounted on top of the second integrated circuit die.

22. A method comprising performing power supply regulation using a sleep transistor.

23. The method of claim 22 further comprising turning off the sleep transistor.

24. The method of claim 22 further comprising sensing a voltage and influencing operation of the sleep transistor with an amplifier in a first control loop.

25. The method of claim 24 further comprising sensing the voltage and influencing the operation of the sleep transistor in a second control loop.

26. An electronic system comprising:

a first integrated circuit including a sleep transistor coupled between a power supply node and a load circuit, the sleep transistor to provide power supply regulation; and

a static random access memory device coupled to the first integrated circuit.

27. The electronic system of claim 26 wherein the first integrated circuit further includes an error amplifier coupled to the sleep transistor.

28. The electronic system of claim 27 wherein the first integrated circuit further includes a multiplexer coupled between the error amplifier and the sleep transistor, wherein the multiplexer is adapted to conditionally turn off the sleep transistor.

29. The electronic system of claim 26 wherein the first integrated circuit further includes a control circuit to conditionally turn off the sleep transistor.

30. The electronic system of claim 29 wherein the control circuit comprises a first control loop including an error amplifier.